REMARKS

Claims 1-18 are pending in this application. Claims 6-10, 17 and 18 are withdrawn from consideration. Claims 1-5 and 11-16 are rejected.

The Invention as set forth in Claims 1-5

The present invention as set forth in amended Claim 1 upon which claims 2-5 depend is directed to a multi-layered semiconductor device which comprises:

1) a film-like semiconductor package as shown in Figs. 2(a), 2(c), 2(e) and 2(f), for example, which incorporates therein a semiconductor chip; and

2) a circuit pattern layer having a package accommodation opening as shown in Figs. 2(b), 2(d) and 2(g).

The semiconductor package is accommodated in the package accommodation opening of the circuit pattern layer and thusly constitute a circuit board. A plurality of the so formed circuit boards are layered together in such a manner that the circuit patterns of the respective circuit boards are electrically connected with each other.

Thus, a small and thin-sized multi-layered semiconductor device, such as a multi-chip module, incorporating therein a number of semiconductor chips, can be obtained. In particular, according to this invention, the semiconductor chip is not directly in the circuit pattern layer, but is incorporated in the semiconductor package at the package accommodation opening of the circuit pattern layer. Therefore, a laminating or layering operation can be effectively carried out and the semiconductor chip can also be protected by the semiconductor package, resulting in an improvement in the reliability of the multi-layered semiconductor device.

According to the present invention, as set forth in Claims 1-5, a multi-layered semiconductor device is produced which has a number of semiconductor chips. The

resulting semiconductor device can also have a relatively complicated wiring or circuit structure. For example, a micro-chip module (MCM) can be obtained according to the present invention. As a result of the present invention, greater efficiencies and yields can be obtained as compared to previous semiconductor devices.

One advantage that the present invention offers is that one can test or individually check the chips before they are incorporated into the semiconductor package thereby saving the time, effort and expense which occurs in the event that a particular semiconductor chip is found to be defective.

The Rejection of Claims 1-5 under 35 U.S.C. 103(a)

The Examiner has rejected Claims 1-5 as allegedly being obvious over U.S. Patent No. 6,335,565 to Miyamoto. Applicants hereby traverse the rejection of the Claims.

In paragraph 4 of page 2 of the Office Action, the Examiner rejected Claims 1-5 under 35 U.S.C. 103(a) as being unpatentable over Miyamoto. As the Examiner admits in the third full paragraph on page 3 of the Office Action, the cited reference fails to teach at least a circuit pattern on the device and it is submitted that the cited reference does not provide any suggestion, motivation or teaching for providing one and arriving at the present invention.

The Office Action states that Miyamoto discloses a multi-layered semiconductor device wherein a semiconductor package incorporates a semiconductor chip to form a circuit board. The Office Action then states that a plurality of such circuit boards are layered together to electrically connect circuit patterns of the respective circuit boards with each other.

Finally, with respect to the Examiner's admission that Miyamoto does not teach a circuit pattern layer, the Office Action states that by flipping the semiconductor package

upside down, the circuit pattern will be on top of the substrate and that therefore, it is not considered inventive to reorient a semiconductor device package. In addition, the Examiner contends that the bump electrodes 4 are part of a circuit pattern, thereby rendering the invention of claim 1 obvious. Applicants respectfully disagree.

It is respectfully submitted that the invention of Miyamoto is directed to an altogether different structure than that of Applicants. The cited portions of Miyamoto, and more particularly Fig. 34, are directed to a structure having a chip AD having leads 5b on one side of the chip. A tape carrier 2b is on leads 5b. Adhesive 10 adheres the bottom of the leads 5b to the top of top tape carrier 2a. In addition, another chip MF has leads 5a which extend underneath bottom tape carrier 2a.

It is respectfully submitted that the above-described structure of Miyamoto, while it does include a plurality of semiconductor chips in a multi-layered device, does not provide a teaching or suggestion to form a circuit layer, as set forth in claim 1, having a package accommodation opening. In other words, applicants claimed invention is the semiconductor packages are not simply layered, but rather the combination of the structures of the semiconductor packages and the circuit pattern layers are layered with respect to each other. Thus, a relatively complicated electrical connection can be attained between the respective packages.

It is respectfully submitted that based on the foregoing, one of ordinary skill in the art would not arrive at the present invention by modifying the Miyamoto reference. Even if one were to modify the structure disclosed in the reference as suggested by the Examiner, the resulting device would not be the claimed invention due to the aforementioned structural differences between the claimed semiconductor device and the device of Miyamoto.

Applicants respectfully request reconsideration of the 35 U.S.C. 103(a) obviousness rejection of Claims 1-5.

The Invention of Claims 11-16

The multi-layered semiconductor device defined by claim 11 is set forth as follows. In the device: 1) a plurality of circuit boards are layered together, wherein each circuit board comprises an insulation substrate, a semiconductor chip incorporated in the substrate, and a circuit formed on a surface of the substrate and electrically connected to the semiconductor chip, and 2) a lead extending from the circuit on the circuit board is bonded, in a through-hole provided in the insulation substrate of the circuit board to a circuit on another circuit board disposed beneath the former circuit board to establish an interlayer connection.

Thus, according to the structure as defined by claim 11, a small and thin-sized semiconductor device, such as a multi-chip module, incorporating therein a number of semiconductor chips, can be obtained.

The Rejection of Claims 11-13, 15 and 16

The Examiner has rejected Claims 11-13, 15 and 16 as allegedly being obvious over U.S. Patent No. 6,335,565 to Miyamoto. Applicants hereby traverse the rejection of the claims 11-13, 15 and 16.

It is respectfully submitted that the portions of the Miyamoto reference cited by the Examiner do not teach nor render obvious the invention of independent Claim 11 and the claims which depend therefrom.

The first full paragraph of the Office Action as stated at the top of page 5 states that the cited portions of Miyamoto referring to the use of polyimide as an insulating substrate render the invention obvious.

It is applicants position that Miyamoto only discloses a plurality of semiconductor packages, each incorporating a semiconductor chip or element forming a multi-layered semiconductor device, but suggest nothing about a particular connecting structure of leads. It is submitted that Miyamoto does not provide a teaching, suggestion or motivation to arrive at the claimed structure of a lead, extending from the circuit on the circuit board, that is bonded, in a through-hole of the insulation substrate of the circuit board, to a circuit on another circuit board to establish an interlayer connection.

Accordingly, it requested that the 35 U.S.C. 103(a) rejection must be withdrawn.

The Rejection of Claim 14 under 35 U.S.C. 103(a)

The Examiner has rejected Claim 14 which is dependent from claim 11 as allegedly being obvious over U.S. Patent No. 6,335,565 to Miyamoto in view of Smith, U.S. Patent Application Publication No. U.S.2001/0001989. Applicants hereby traverse the rejection of the claim.

It is respectfully submitted that the proffered combination of references cannot render the rejected claims obvious because the secondary Smith reference does not provide the teaching noted above with respect to the above-described features which are absent from the primary Miyamoto reference. Smith is cited in the Office Action for the purposes of showing a disclosure of beam lead bonding for electrically connecting a chip to a circuit board. However, there is no suggestion in Smith of a lead extending from the circuit on the circuit board, that is bonded, in a through-hole of the insulation substrate of the circuit board, to a circuit on another circuit board to establish an interlayer connection.

It is also submitted that Smith suggests nothing about a structure of a multi-layered semiconductor device incorporating therein a semiconductor chip. In fact, Smith suggests nothing regarding an electrical connection between circuit boards which are layered.

Thus, the combination of the cited references fails to teach or suggest all the claim limitations.

It is also submitted that the Examiner's rejection of the claims involves the use of improper hindsight. Applicants note that the Smith reference was published May 31, 2001 and filed January 10, 2001 which is substantially after the priority date of the present application (Japanese Patent Application No. 2000-191090 filed on June 21, 2000). To prevent the use of hindsight based on the invention to defeat patentability of the invention, the courts require the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet, 47* USPQ 2d *1453, 1457-58* (Fed. Cir. 1998*)*. Accordingly, it is respectfully submitted that the proposed combination of references is the product of improper hindsight.

Based on the reasoning stated above, Applicant believes one of ordinary skill in the art would not arrive at the present invention by combining Miyamoto with Smith. Therefore, reconsideration of the rejection of Claim 14 and its allowance is respectfully requested.

CONCLUSION

For the reasons set forth above, Applicants' present invention, as recited in the amended claims now more clearly and particularly, is patentable. Reconsideration and withdrawal of all outstanding rejections in this case is hereby respectfully requested.

If further matters remain in connection with this case, the Examiner is invited to telephone the Applicant's undersigned representative to resolve them.

Respectfully submitted,

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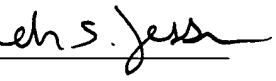

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